Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **BAL/COMP**
2. **INPUT –**
3. **INPUT +**
4. **V –**
5. **BALANCE**
6. **OUTPUT**
7. **V +**
8. **COMP**

**.047”**

**.046”**

**1 2 3**

**6**

**7**

**8**

**4**

**5**

**DIE ID**

**L**

**M**

**1**

**0**

**1**

**F**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V-**

**Mask Ref: LM101 F**

**APPROVED BY: DK DIE SIZE .046” X .047” DATE: 10/4/22**

**MFG: NATIONAL THICKNESS .014” P/N: LM101A**

**DG 10.1.2**

#### Rev B, 7/19/02